REMARKS

Claim 55 has been amended. No claims have been cancelled. No new claims have been added. Thus, claims 1-71 are pending.

Applicant acknowledges that the Office Action states that the documents listed under the "Other Prior Art – Non Patent Literature" category of the IDS file on April 22, 2003 were not considered because the Examiner did not find copies of these documents. The IDS was filed with copies of each document cited in the IDS, but the document were contained in a separate box, which apparently was separated from the file by the PTO. A copy of the postcard filing receipt acknowledging PTO receipt of the references is attached. In response, a copy of the previously filed IDS listing the previously non-considered documents is being submitted again together with another copy of each document.

Applicant's representative gratefully acknowledges the indication of allowable subject matter in claims 5-6, 8-9, 12, 17-24, 29-32, 38, 40-41, 44, 48-51, 53-54, 58-61, 65, 67-68, and 71.

Claims 1-4, 7, 10-11, 13-16, 25-28, 33-37, 42-43, 45-47, 52, 55-57, 62-64, 66, and 69-70 stand rejected under 35 U.S.C. 102(a) as being anticipated by Lowrey (WO 01/45108-A1). This rejection is respectfully traversed.

The present invention is directed to a method and apparatus for writing data to a programmable conductor random access memory (PCRAM) cell. Accordingly, each of the independent claims recites a method or apparatus for writing or programming a memory cell. More specifically, independent claim 1 recites: "A method for writing to a memory element, said method comprising: ... coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element. Independent claim 13 recites: "A method for writing a semiconductor memory cell, the method comprising: ... using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element." Independent claim 25 recites: "... connecting a second

terminal of said chalcogenide memory element to said bit line to produce a voltage across said memory element sufficient to write a predetermined resistance state into said memory element." Independent claim 35 recites: "... said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state." Independent claim 45 recites: "... an access transistor responsive to a voltage on a word line for selectively coupling said bit line to said second terminal of said memory element to program said memory element to a resistance state based on the voltage values on said cell plate and bit line." Independent claim 55 recites: "... said device causing a voltage to be applied across said chalcogenide memory element sufficient to write one of two predetermined resistance states in said chalcogenide element depending on which of said first or second voltage is precharged on said memory line." Finally, independent claim 62 recites: "... said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state."

Lowrey discloses a memory system comprising a plurality of memory cells and reference cells. The memory cells of Lowrey are programmable resistance memory cells based on phase change material. The Office Action alleges that Lowrey discloses the claimed invention by disclosing a precharging of a column line at page 16, lines 14-15, holding the precharged voltage on the column line at page 17, lines 8-9, and coupling a programmable conductor memory element M between a first and second voltage at Fig. 3. However, a closer examination of Lowrey reveals that the passages cited by the Office Action relate to a method and mechanism for reading the memory cells of Lowrey. For example, pages 16 – 17 of Lowrey is exclusively directed to a method for reading a memory cell M having the structure as shown in Fig. 3. Indeed, Lowrey, at page 17, line 6-7 state "As discussed above, this is done to prevent the memory element from changing resistance states as a result of the read operation" (emphasis supplied). Further, page 17, lines 8-10 merely states that "[t]he time needed to charge a column line is directly proportional to the capacitance of the column line as well as the resistance of the

corresponding programmable resistance element M coupled to the column line." Indeed, the only portion of Lowrey which appears to discuss writing a memory cell appears to be at page 33, lines 7-11, which states: "The programmable resistance element may be directly overwritable so that it can be programmed to a specific resistance state (for example, the first or the second resistance state) without the need to first be programmed to any starting state. The programmable resistance element may be a programmable resistor." It is respectfully submitted that Lowrey fails to disclose or suggest the above recited limitations of the independent claims.

Thus, claims independent claims 1, 13, 25, 35, 45, 55, and 62 are believed to be allowable over the prior art of record. The depending claims (2-12, 14-24, 26-34, 36-44, 46-53, 56-61, and 63-71) are also believed to be allowable for at least the same reasons as their respective independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By_____

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